UNIT-1

Introduction to semiconductor memories and technologies
Overview

- Basic memory circuits
- Organization of the main memory
- Cache memory concept
- Virtual memory mechanism
- Secondary storage
Some Basic Concepts
Basic Concepts

- The maximum size of the memory that can be used in any computer is determined by the addressing scheme. 
  16-bit addresses = $2^{16} = 64$K memory locations
- Most modern computers are byte addressable.

<table>
<thead>
<tr>
<th>Word address</th>
<th>Byte address</th>
<th>Byte address</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0 1 2 3</td>
<td>0 3 2 1 0</td>
</tr>
<tr>
<td>4</td>
<td>4 5 6 7</td>
<td>4 7 6 5 4</td>
</tr>
</tbody>
</table>

(a) Big-endian assignment  
(b) Little-endian assignment
Figure 5.1. Connection of the memory to the processor.
Basic Concepts

- “Block transfer” – bulk data transfer
- Memory access time
- Memory cycle time
- RAM – any location can be accessed for a Read or Write operation in some fixed amount of time that is independent of the location’s address.
- Cache memory
- Virtual memory, memory management unit
Semiconductor RAM Memories
Internal Organization of Memory Chips

16 words of 8 bits each: 16x8 memory org.. It has 16 external connections: addr. 4, data 8, control: 2, power/ground: 2

1K memory cells: 128x8 memory, external connections: ? 19(7+8+2+2)

1Kx1: ? 15 (10+1+2+2)

Figure 5.2. Organization of bit cells in a memory chip.
Memory Cell Operations

(a) Write
(b) Read
The Basic Elements: Memory Cells

- Memory cell properties
  - two stable states for representing binary 1 and 0
  - can be written into at least once to set the state
  - can be read to sense the state
Semiconductor Memory Types

(Internal and Random Access)

Read-write memory

Read-only memory

Read-mostly memory

Random-access memory (RAM)

- Static RAM (SRAM)
- Dynamic RAM (DRAM)
  - Synchronous DRAM (SDRAM)
  - Rambus DRAM (RDRAM)
  - Cache DRAM (CDRAM)

Read-only Memory (ROM)

Programmable ROM (PROM)

Erasable PROM (EPROM)

Electrically Erasable PROM (EEPROM)

Flash memory
# Classification of Memories

<table>
<thead>
<tr>
<th>RW Memory</th>
<th>NVRWM</th>
<th>ROM</th>
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<tbody>
<tr>
<td>Random Access</td>
<td>Non-Random Access</td>
<td>EPROM, EEPROM, FLASH</td>
</tr>
<tr>
<td>SRAM (Static)</td>
<td>FIFO (Queue)</td>
<td>Mask Programmed</td>
</tr>
<tr>
<td>DRAM (Dynamic)</td>
<td>LIFO (Stack)</td>
<td>PROM (Fuse Programmed)</td>
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<td></td>
<td>SR (Shift Register)</td>
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<td>CAM (Content Addressable)</td>
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## Trends in Storage Technology

### SRAM

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<tbody>
<tr>
<td>$/MB</td>
<td>19,200</td>
<td>2,900</td>
<td>320</td>
<td>256</td>
<td>100</td>
<td>190</td>
</tr>
<tr>
<td>access (ns)</td>
<td>300</td>
<td>150</td>
<td>35</td>
<td>15</td>
<td>2</td>
<td>100</td>
</tr>
</tbody>
</table>

### DRAM

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<tr>
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</thead>
<tbody>
<tr>
<td>$/MB</td>
<td>8,000</td>
<td>880</td>
<td>100</td>
<td>30</td>
<td>1</td>
<td>8,000</td>
</tr>
<tr>
<td>access (ns)</td>
<td>375</td>
<td>200</td>
<td>100</td>
<td>70</td>
<td>60</td>
<td>6</td>
</tr>
<tr>
<td>typical size(MB)</td>
<td>0.064</td>
<td>0.256</td>
<td>4</td>
<td>16</td>
<td>64</td>
<td>1,000</td>
</tr>
</tbody>
</table>

### Disk

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<tr>
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</thead>
<tbody>
<tr>
<td>$/MB</td>
<td>500</td>
<td>100</td>
<td>8</td>
<td>0.30</td>
<td>0.05</td>
<td>10,000</td>
</tr>
<tr>
<td>access (ms)</td>
<td>87</td>
<td>75</td>
<td>28</td>
<td>10</td>
<td>8</td>
<td>11</td>
</tr>
<tr>
<td>typical size(MB)</td>
<td>1</td>
<td>10</td>
<td>160</td>
<td>1,000</td>
<td>9,000</td>
<td>9,000</td>
</tr>
</tbody>
</table>

*MB=Mbytes
Increasing die size factor 1.5 per generation
Combined with reducing cell size factor 2.6 per generation
Non volatile memory

- EEPROM – electrically erasable memory, a general-term
  - this is a historical term to differentiate from an older type of memory that used UV-light to for eraser
- “Flash” memory is the dominant type currently
  - NOR flash
  - NAND flash
- A relatively recent new type of non-volatile Memory is MRAM – Magnetoresitive Random